CHIPMAT

COMMERCIALISATION GRANT

Validation and Commercialisation Support for Semiconductor Design, Advanced Materials and Application Development with Indigenous Chips

GRANT SUPPORT OF UP TO ₹40 LAKH PER PROJECT

Implemented jointly by the Maker Hub and Atal EIC

CALL FOR APPLICATIONS • PROGRAM GUIDELINES • APPLICATION FORMAT

Document at a Glance

Program name	CHIPMAT Commercialisation Grant
Grant ceiling	Up to ₹40 lakh per selected project
Project period	Normally 9–18 months
Focus	Three verticals: semiconductor design and allied areas; advanced materials and allied areas; application development with indigenous chips
Maturity sought	Technologies beyond basic proof of concept, normally TRL 4 or above
Primary outcomes	Independent validation, application integration, pilot deployment, qualification, manufacturing readiness and commercial traction
Implementing institutions	Maker Hub / IIITMK and Atal EIC
Call mode	Competitive, milestone-based and subject to technical and commercial due diligence
Equity consideration	For each grant awarded, IIITMK will receive a flat 2% equity stake in the selected company.
Portfolio size	A maximum of 20 companies will be supported under the scheme.

Program proposition

CHIPMAT bridges the gap between a technically promising prototype and a commercially deployable product, process, design IP, material platform or indigenous-chip-based application. The grant is intended to pay for the high-risk validation work that customers and investors expect, but early-stage ventures often cannot finance.

Contents

1. Call for Applications

The Maker Hub and Atal EIC invite applications for the CHIPMAT Commercialisation Grant from Indian startups, research spin-outs, MSMEs and technology teams developing commercially relevant innovations across three verticals: semiconductor design and allied areas; advanced materials and allied areas; and application development with indigenous chips.

Selected projects may receive milestone-based grant support of up to ₹40 lakh for a period normally ranging from 9 to 18 months. The program is aimed at technologies that have moved beyond the concept stage and require engineering validation, fabrication, application integration, testing, qualification, pilot deployment, customer acceptance or manufacturing-readiness support. A maximum of 20 companies will be supported under the scheme. For each grant awarded, IIITMK will receive a flat 2% equity stake in the selected company, as documented in the grant agreement.

What CHIPMAT is designed to achieve
A credible transition from proof of concept to market: validated performance, repeatable engineering, an identified user or customer, a manufacturing, deployment or licensing pathway, and evidence capable of supporting procurement, investment or larger national funding.

1.1 Who should apply?

- A fabless semiconductor startup requiring design closure, verification, MPW/tapeout, packaging or test support.
- A semiconductor-enabled product company with proprietary circuit, device, packaging, sensor or system IP requiring independent validation or customer pilots.
- An advanced-materials venture requiring process optimisation, repeatability studies, application integration, pilot-batch production or customer qualification.
- An application-development venture building deployable products, reference designs, embedded systems or sector solutions around indigenous chips, and requiring hardware integration, firmware, system validation, certification or customer-pilot support.
- A research team or spin-out with defensible IP and a committed plan to incorporate and commercialise.
- An MSME developing a genuinely new, high-risk semiconductor, advanced-material or indigenous-chip-based application, product or process.

1.2 What will not be supported?

- Basic research or academic studies without a defined product, process, IP or market outcome.
- Concept-only proposals without preliminary technical evidence.
- Routine customisation, contract engineering, trading, reselling or general software services not materially tied to the deployment of indigenous chips.
- Full-scale fabrication plants, production lines, buildings or other major capital projects.
- Work already fully financed through another public or private grant.

2. Program Context and Rationale

Semiconductor-design, advanced-material and indigenous-chip application ventures face a difficult commercialisation gap. Even after proof of concept, they must finance specialised design tools, fabrication runs, packaging, testing, material characterisation, board and system integration, firmware or driver development, repeatability studies, reliability assessment, qualification and customer pilots. These activities are expensive, technically uncertain and often occur before meaningful revenue or institutional investment.

The Maker Hub brings experience in hardware incubation, prototyping, technology translation and startup support. Atal EIC contributes structured incubation, grant administration, business development, investor engagement and commercialisation support. CHIPMAT combines these capabilities into a focused validation-to-market mechanism.

The program is aligned with a design-led semiconductor ecosystem in which shared tools, labs, fabrication access, packaging and testing networks, indigenous-chip evaluation platforms, application engineering, customer pilots, intellectual-property support and commercial linkages are used to create indigenous chips, materials, products and high-value ventures.

3. Objectives and Intended Outcomes

- Accelerate promising semiconductor-design, advanced-material and indigenous-chip application technologies toward commercial deployment.
- Generate independent evidence of product, process, material, design or application-system performance.
- Support fabrication, packaging, characterisation, application engineering, system integration, qualification and pilot deployment.
- Improve manufacturability, repeatability, reliability, cost and supply-chain readiness.
- Help ventures secure customers, licensing partners, strategic investors and follow-on grants.
- Promote indigenous IP, import substitution and high-value technical employment.
- Create a pipeline for larger national and sectoral semiconductor, electronics, deep-tech and manufacturing programs.

3.1 Mandatory end-of-project position

Every funded project must finish with a defined commercial decision point. Depending on the project, this may be a validated chip or IP block, qualified material, indigenous-chip-based application, reference design, customer-evaluation batch, field-tested system, pilot deployment, manufacturing-transfer package, licence-ready technology, purchase commitment, investment-ready data room or a larger scale-up proposal.

4. Focus Areas

4.1 Semiconductor Design and Allied Areas

- Analog, mixed-signal, digital, RF, microwave and millimetre-wave ICs.
- ASICs, SoCs, RISC-V processors, accelerators, FPGA-to-ASIC transitions and reusable semiconductor IP.
- Power-management ICs, power devices and solutions based on silicon, SiC, GaN or other wide-bandgap platforms.
- MEMS, NEMS, smart sensors, sensor interfaces and semiconductor-enabled instrumentation.
- Edge AI, neuromorphic computing, hardware security, secure elements and cryptographic accelerators.
- Silicon photonics, optoelectronics, photonic integrated circuits and related control electronics.
- Chiplets, advanced interconnects, heterogeneous integration, packaging and thermal-management solutions.
- Verification, physical design, design-for-test, EDA automation, test engineering and reliability technologies.
- Application-specific semiconductor devices, chipsets and subsystem IP for health, mobility, energy, telecom, industrial, defence, space, agriculture and environmental monitoring.

4.2 Advanced Materials and Allied Areas

- Electronic, dielectric, ferroelectric, piezoelectric, magnetic and optoelectronic materials.
- Graphene, two-dimensional materials, nanomaterials, thin films, coatings and engineered interfaces.
- Wide-bandgap and ultra-wide-bandgap semiconductor materials and related processes.
- Flexible, printed, wearable and stretchable electronics; conductive inks and additive-electronics materials.
- Advanced substrates, interposers, encapsulants, underfills, adhesives and packaging materials.

- Thermal-interface, heat-spreading and heat-dissipation materials.
- Semiconductor-grade chemicals, precursors, gases, photoresists, wafers, targets and high-purity consumables.
- Photonic, quantum, sensing and spintronic materials.
- Materials for energy storage, hydrogen, fuel cells, supercapacitors and energy harvesting where linked to electronics or semiconductor applications.
- Material recovery, recycling, process sustainability, waste reduction and circular semiconductor technologies.
- Material-characterisation instrumentation, process-control tools and AI-assisted material or process optimisation.

4.3 Application Development with Indigenous Chips

- Embedded, edge-AI, IoT and cyber-physical products built around indigenous processors, microcontrollers, ASICs, FPGAs, sensors, power devices, secure elements or chipsets.
- Reference designs, evaluation platforms, modules, boards, controllers, gateways, instruments and sector-specific systems that accelerate adoption of indigenous chips.
- Application hardware, PCB design, firmware, device drivers, board-support packages, middleware, toolchains and system software required to deploy indigenous chips.
- Porting and optimisation of existing applications for indigenous chips, including performance, power, security, safety, reliability and interoperability.
- Qualification, certification, manufacturing readiness, customer pilots and field deployment of indigenous-chip-based applications in healthcare, mobility, EVs, energy, telecom, industry, defence, space, agriculture, fisheries and environmental monitoring.

4.4 Priority themes

- Indigenous alternatives to strategically imported components, materials or process inputs.
- Technologies with an identified pilot customer or industry collaborator.
- Applications that create demonstrable demand, reference use cases and repeatable market adoption for indigenous chips.
- Products capable of measurable impact in healthcare, EVs, energy, defence, space, telecom, agriculture, fisheries, environment or industrial automation.
- Energy-efficient, sustainable or circular technologies.
- Projects capable of achieving a clear commercial milestone within 18 months.

5. Applicant and Project Eligibility

5.1 Eligible applicants

- DPIIT-recognised startups and Indian incorporated companies or LLPs.
- Product and application-development companies building deployable hardware, embedded systems, reference platforms or sector solutions around indigenous chips.
- MSMEs undertaking a new, high-risk semiconductor, advanced-material or indigenous-chip application-development project.
- Faculty-led, researcher-led, student-led or alumni-led teams that will incorporate an Indian entity before grant disbursement.
- Joint teams involving a startup and an academic institution, R&D laboratory or industry partner.
- Technology-transfer or licensing ventures with documented rights to commercialise the proposed IP.

5.2 Minimum project readiness

Projects should normally be at Technology Readiness Level 4 or above. Applicants must provide evidence of technical feasibility, such as simulation results, laboratory data, initial samples, functional boards, FPGA prototypes, application prototypes, board bring-up, firmware or driver demonstrations, preliminary design files, device measurements, process results, patent filings, chip-access evidence or third-party test reports.

5.3 Essential conditions

- At least one core technical founder or project lead must remain substantially engaged.
- The applicant must disclose all prior and current grants, investments and overlapping project support.
- Background IP, institutional ownership and third-party restrictions must be clearly documented.
- Application-development proposals must identify the indigenous chip(s), show access or active engagement with the chip developer/supplier, and demonstrate that the proposed work materially advances deployment and adoption.
- The proposed milestones must be achievable within the grant period and budget.
- Applicants must be able to maintain project accounts, records, utilisation evidence and technical documentation.
- Selected applicants must agree to provide IIITMK with a flat 2% equity stake as a condition of the grant award.

6. Grant Structure and Financial Support

Grant ceiling
Up to ₹40 lakh per selected project. The sanctioned amount will depend on technical maturity, validation scope, fabrication, application-development or pilot requirements, commercial potential, budget justification and committee recommendations.

Equity and portfolio cap
For each grant awarded, IIITMK will receive a flat 2% equity stake in the selected company. A maximum of 20 companies will be supported under the scheme.

6.1 Duration

The project period will normally be 9 to 24 months. Shorter or longer periods may be approved only where fabrication cycles, application-integration or qualification protocols, or external facility schedules justify them.

6.2 Indicative milestone tranches

Tranche	Indicative share	Trigger	Illustrative evidence
1	30%	Grant agreement and approved execution plan	Detailed milestones, quotations, baseline data and vendor plan
2	30%	Completion of first technical milestone set	Design review, sample data, application-integration evidence, prototype evidence or process results
3	25%	Prototype/fabrication/application-integration/pilot-batch milestone	Chip, packaged device, validated material, indigenous-chip application, integrated prototype or pilot batch

Tranche	Indicative share	Trigger	Illustrative evidence
4	15%	Final validation and commercialisation milestone	Independent report, customer feedback, manufacturing and market-entry plan

The committee may modify the tranche pattern for projects with large external vendor payments. Payments for foundry access, MPW participation, packaging, application-integration services, testing, certification or specialised facilities may be made directly to approved service providers.

6.3 Equity consideration and portfolio size

For each grant awarded, IIITMK will receive a flat 2% equity stake in the selected company. This condition will be documented in the grant agreement and related equity documentation. The scheme will support a maximum of 20 companies in total.

7. Supported and Non-supported Expenditure

7.1 Permitted expenditure

- EDA tools, project-specific software, firmware-development tools, cloud computing, design IP and verification resources.
- FPGA boards, evaluation kits, PCB fabrication, electronic components and application boards.
- Application hardware, PCB and module development, board bring-up, firmware, device drivers, board-support packages, middleware, toolchain integration, porting and optimisation for indigenous-chip deployment.
- MPW, mask, foundry, wafer-processing, tapeout, packaging, assembly and test costs.
- Material synthesis, formulation, process optimisation, prototype tooling and pilot-batch expenses.
- Wafers, substrates, targets, chemicals, precursors, consumables and sample preparation.
- Laboratory, cleanroom, characterisation and reliability-facility access.
- Third-party testing, calibration, certification, qualification and regulatory work.
- Project-specific engineering, research and technical manpower.
- Specialist consultants for design, process, embedded systems, firmware, application integration, packaging, test, reliability, DFM or standards.
- Patent search, Indian patent filing, IP documentation and licensing preparation.
- Customer pilots, field trials, application engineering, product engineering and manufacturing-readiness work.
- Travel directly associated with fabrication, testing, technical collaboration or customer validation.

7.2 Expenditure limits and controls

- Project-specific manpower should ordinarily not exceed 30% of the sanctioned grant unless specially approved.
- Equipment purchases must be essential, project-specific and justified against rental or shared-facility access.
- All major external expenses must be supported by quotations or a documented procurement basis.
- Related-party procurement must be disclosed and requires prior approval.
- Expenditure incurred before the grant start date will not normally be reimbursed.

7.3 Non-permitted expenditure

- Land, buildings, civil works, vehicles and general office infrastructure.
- Loan repayment, historical liabilities, dividends or unrelated founder remuneration.
- General marketing, advertising, sales commissions or routine business development.
- Large-scale commercial production machinery or full manufacturing facilities.

- Routine consulting, trading, contract services, standalone software development not materially dependent on indigenous chips, or unrelated product development.
- Activities already fully supported by another grant.

8. Application and Selection Process

Stage 1 — Application: Submission of technical, commercial, financial, IP and team information in the prescribed format.

Stage 2 — Eligibility screening: Review of thematic fit, legal eligibility, maturity, completeness and overlap with other funding.

Stage 3 — Domain evaluation: Assessment by semiconductor, materials, embedded-system, application-engineering, product, manufacturing and commercial experts.

Stage 4 — Diagnostic interaction: Technical clarification, milestone refinement, customer validation review and budget rationalisation.

Stage 5 — Pitch and due diligence: Presentation to the Grant Selection and Review Committee and verification of claims, ownership, quotations and partner commitments.

Stage 6 — Approval and contracting: Issue of sanction, execution of the milestone-based grant agreement and related documentation for IIITMK's flat 2% equity stake, and project commencement.

8.1 Required application package

1. Executive summary and problem statement.
2. Technology description, architecture, process flow or indigenous-chip application stack.
3. Current maturity and evidence of feasibility.
4. Validation and commercialisation plan.
5. Milestones, deliverables, timeline and risk plan.
6. Customer, end-user, indigenous-chip provider or industry engagement evidence.
7. Competitive landscape and quantified differentiation.
8. IP ownership, patent status and freedom-to-operate position.
9. Manufacturing, fabrication, packaging, application integration, testing, deployment or scale-up pathway.
10. Detailed budget with quotations.
11. Team profiles and project responsibilities.
12. Funding history, cap table and conflict-of-interest disclosures.

9. Evaluation Framework

Criterion	Weight	Key questions
Technical innovation and differentiation	15%	Is the solution meaningfully better, defensible and technically credible?
Existing maturity and evidence	15%	Has feasibility been demonstrated with relevant data?
Validation plan	15%	Will the proposed work remove the key adoption risks?
Commercial need and market opportunity	15%	Is there a clear use case, customer pain point and addressable market?
Customer or industry engagement	10%	Are users, pilots, evaluators or partners identified?

Criterion	Weight	Key questions
Milestones and budget	10%	Are outputs measurable, realistic and cost-effective?
Team capability and commitment	10%	Can the team execute the technical and commercial plan?
IP and competitive position	5%	Are ownership and protection credible?
Manufacturing/deployment/licensing/scale-up potential	5%	Is there a realistic route beyond the grant?

9.1 Selection principles

- Selection will not be based solely on presentation quality or projected market size.
- Technical and commercial thresholds may be applied independently.
- The committee may approve a lower amount, narrower scope or revised milestone plan.
- Portfolio balance across semiconductor design, advanced materials, indigenous-chip application development, application sectors and maturity may be considered.
- For the third vertical, evaluation will consider the materiality of indigenous-chip use, depth of technical integration and potential for repeatable adoption.
- All reviewers must disclose conflicts of interest and recuse themselves where required.

10. Project Monitoring and Disbursement

- Kick-off review and baseline documentation.
- Monthly progress updates and quarterly formal reviews.
- Technical design, sample, prototype, application-integration or process demonstrations.
- Financial statements, invoices, procurement records and utilisation certificates.
- Independent technical testing or expert review where required.
- Customer-pilot and commercialisation progress reports.
- Final technical dossier, commercialisation plan and audited utilisation statement.

10.1 Committee powers

Based on progress, the review committee may approve the next tranche, require corrective action, revise milestones, reallocate approved budget heads, defer disbursement, reduce the sanctioned amount or terminate the project. Material non-performance, misrepresentation, diversion of funds or undisclosed duplicate funding may trigger recovery provisions.

11. Technical and Commercial Support

11.1 Technical support

- Design reviews, architecture reviews, application and system reviews, and manufacturability diagnostics.
- Access or connections to EDA, FPGA, PCB, embedded-system, software-porting and prototyping facilities.
- Connections to indigenous-chip developers, evaluation platforms, SDKs, board-support packages and application-enablement networks.
- Foundry, MPW, packaging, test, reliability and certification networks.
- Material synthesis, processing, characterisation and pilot-scale partner facilities.
- Experts in circuit design, devices, materials, embedded systems, firmware, application engineering, packaging, thermal management, testing and standards.

11.2 Commercial support

- Customer discovery, use-case refinement and pilot structuring.
- Corporate, government, indigenous-chip developer and industry introductions.
- Pricing, business model, licensing and go-to-market support.
- Supply-chain, manufacturing, deployment and technology-transfer planning.
- Investor readiness, data-room preparation and follow-on funding support.
- Applications to larger national, sectoral or strategic programs.

11.3 IP and legal support

- Prior-art and patentability guidance.
- Indian patent-filing and IP documentation support.
- Founder, institutional, licence and technology-transfer agreements.
- Confidentiality, pilot, evaluation and collaboration agreements.
- Support in defining background IP and project-generated foreground IP.

12. Governance, IP and Compliance

12.1 Governance structure

Program Steering Committee	Strategic priorities, annual budget, policy approvals, partnerships and impact review.
Grant Selection and Review Committee	Selection, milestone approval, technical/commercial review and corrective decisions.
Program Management Unit	Call administration, contracting, monitoring, finance, documentation and portfolio support.
Domain Expert Panels	Specialist review for semiconductor design, devices, advanced materials, embedded systems, application engineering, packaging and testing.

12.2 Roles of the implementing partners

Maker Hub: Technical infrastructure, engineering support, prototyping, indigenous-chip integration, application and system reviews, facility/vendor coordination and technology monitoring.

Atal EIC: Grant administration, incubation, business support, financial compliance, mentor and investor engagement, IP facilitation and commercialisation.

Joint responsibilities: Call management, committee constitution, grant approval, industry and academic partnerships, progress reviews, outcome reporting and resource mobilisation.

12.3 Intellectual-property principles

- Background IP remains with its pre-project owner.
- Foreground IP generated by the applicant will ordinarily remain with the applicant.
- Where an institution or third party is involved, rights must be documented before major disbursement.
- For each grant awarded, IIITMK will receive a flat 2% equity stake in the selected company, subject to the grant agreement and related equity documentation.
- The program may publicly showcase non-confidential information with the grantee's consent.
- Applicants must disclose licences, assignments, institutional claims and third-party restrictions.

12.4 Compliance

- Grant agreement, milestone schedule and approved budget.
- Execution of the documentation required to provide IIITMK with the flat 2% equity stake.
- Separate accounting records and traceable expenditure documentation.
- Conflict-of-interest and related-party disclosure.
- Confidentiality, data and information-security obligations.
- Applicable tax, labour, environmental, safety and regulatory compliance.
- Audit, inspection, record-retention and recovery provisions.

13. Program Timeline and KPIs

Processed every month

13.1 Indicative program KPIs

- Number of validated semiconductor designs, IP blocks, devices, materials, processes, indigenous-chip applications, reference designs or systems.
- MPW/tapeout, packaging, application-integration, testing and qualification outcomes.
- Independent technical-validation reports and reliability datasets.
- Customer pilots, evaluation batches, indigenous-chip deployments and field trials.
- Number and diversity of indigenous chips adopted in funded applications.
- Patents, process know-how packages, licences and technology transfers.
- Purchase commitments, commercial revenue or paid development engagements.
- Follow-on grants, strategic investments and industry co-development.
- High-value technical jobs and indigenous supply-chain opportunities.
- A supported portfolio capped at a maximum of 20 companies under the scheme.

14. Application Form

Submission note
Applicants should respond clearly and provide evidence. Unsupported claims, incomplete IP disclosures or unrealistic milestone plans may lead to rejection.

A. Applicant Details

Legal name of applicant entity/team:

_____

Registered office and website:

_____

Entity type and incorporation date:

_____

DPIIT/MSME/other registration details:

_____

Primary contact name, designation, email and phone:

_____

Founders/promoters and shareholding:

_____

Academic/R&D/industry partners, if any:

_____

B. Project Overview

Project title:

_____

Track: Semiconductor Design / Advanced Materials / Application Development with Indigenous Chips

_____

Grant amount requested:

_____

Proposed duration:

_____

Current TRL and target TRL:

_____

For Application Development with Indigenous Chips, identify the chip(s), chip developer/supplier and current access/integration status:

_____

One-sentence value proposition:

_____

Target application sector and primary customer/user:

C. Problem and Market Need

Describe the customer or industry problem.

Who experiences the problem, and how is it addressed today?

Provide evidence of demand, customer discovery or pilot interest.

Estimate the relevant market and initial reachable segment.

D. Technology and Differentiation

Describe the product, design IP, device, material, process, application or platform.

Summarise the architecture, process flow, indigenous-chip integration stack or scientific principle.

Provide current performance and supporting evidence.

Compare against the most relevant alternatives.

Explain the technical advantage and barriers to replication.

E. Validation and Commercialisation Plan

State the key technical and adoption risks to be removed.

List proposed validation, fabrication, packaging, application-engineering, integration, testing or pilot activities.

Identify indigenous-chip developers/suppliers, external facilities, vendors and partners.

Describe the customer pilot or evaluation plan.

State the expected commercial decision at project completion.

F. Intellectual Property

Background IP owner(s):

Patents filed/granted and jurisdictions:

Institutional, licence or third-party rights:

Freedom-to-operate work completed or planned:

Foreground IP expected from the project:

G. Manufacturing, Deployment and Scale-Up

Proposed fabrication/manufacturing/deployment route:

Key chip developers/suppliers, foundries, OSATs, labs, manufacturers or integration partners:

Expected unit economics or techno-economic position:

Quality, certification, safety or regulatory requirements:

Scale-up risks and mitigation:

H. Team

Core team members, roles and time commitment:

Relevant technical and commercial experience:

Critical skills currently missing:

Planned hiring or specialist support:

I. Funding and Commercial History

Grants received or applied for:

Equity/debt funding received:

Revenue, pilots, purchase orders or licences:

Any overlapping funding for the proposed activities:

_____

J. Milestone Plan

No.	Milestone	Activities	Deliverable	Evidence	Month	Budget (₹)
1						
2						
3						
4						
5						

K. Detailed Budget

Budget head	Description/vendor	Amount (₹)	Quotation attached	Justification
EDA/software/firmware/IP				
Fabrication/tapeout				
Packaging/testing/integration				
Materials/consumables				
Facility access				
Manpower				
Consultants				
IP/certification				
Pilot/travel				

L. Risk Register

Risk	Probability	Impact	Mitigation	Owner

15. Annexures and Declarations

Annexure 1 — Documents Checklist

- ☐ Certificate of incorporation or undertaking to incorporate.
- ☐ DPIIT/MSME registration, where applicable.
- ☐ Founder and core-team profiles.
- ☐ Technical evidence: reports, data, simulations, photographs, designs, boards, firmware/integration results or characterisation.
- ☐ IP documents, patent filings, licences and institutional permissions.
- ☐ Customer letters, indigenous-chip provider confirmations, pilot commitments or industry-partner letters.
- ☐ Major vendor quotations and facility estimates.
- ☐ Financial statements or management accounts, where available.
- ☐ Cap table and details of existing investors.
- ☐ Details of grants and other public funding.
- ☐ Board/authorised-signatory approval for submission.

Annexure 2 — Applicant Declaration

We certify that the information provided in this application is true and complete to the best of our knowledge. We have disclosed all material information regarding ownership, intellectual property, grants, investments, related parties, conflicts of interest and overlapping support. We understand that selection does not create an entitlement to the maximum grant amount and that disbursement will be subject to due diligence, contracting, milestones and availability of funds. We acknowledge and agree that, for any grant awarded under this scheme, IIITMK will receive a flat 2% equity stake in the applicant company through the grant agreement and related equity documentation. We agree to maintain records, permit technical and financial review, use funds only for approved purposes and promptly report any material change affecting the project.

Name of authorised signatory	
Designation	
Applicant entity	
Place and date	
Signature and seal	

Annexure 3 — Suggested Final Project Dossier

- Executive completion summary.
- Milestone-wise technical report and evidence.
- Design files, application hardware/firmware/software files, test data, material/process records and version history, as applicable.
- Independent test, characterisation, reliability or qualification reports.
- Customer-pilot report and feedback.
- IP created and filings made.
- Manufacturing, deployment, licensing and commercialisation plan.
- Budget utilisation and asset/consumable statement.
- Follow-on funding, partnership and revenue pipeline.
- Lessons, risks and next-stage resource requirements.

Contact and Submission

Application channel
Applications should be submitted through the official call portal or to the email address notified in the public announcement. The final call notice should specify the opening date, closing date, help-desk contact, briefing-session schedule and permitted file formats.

CHIPMAT COMMERCIALISATION GRANT

Design. Integrate. Validate. Qualify. Pilot. Commercialise.